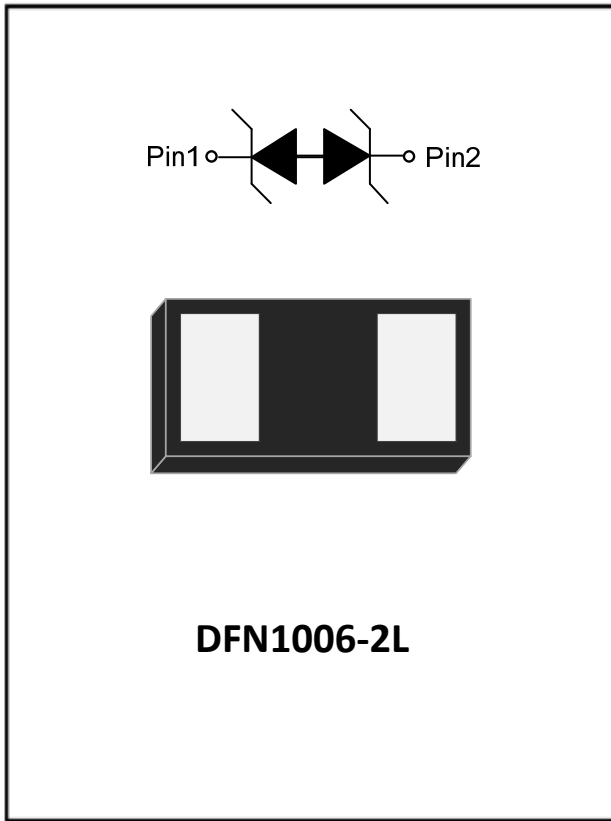


1-Line, Bi-directional, Ultra-low Capacitance Transient Voltage Suppressor



Features

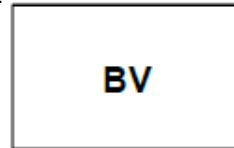
- Stand-off voltage: 5V Max
- Transient protection for each line according to
IEC61000-4-2(ESD): $\pm 20\text{kV}$ (contact)
IEC61000-4-5(surge): 3A (8/20 μs)
- Ultra-low leakage current
- Ultra low clamping voltage
- RoHS Compliant

Applications

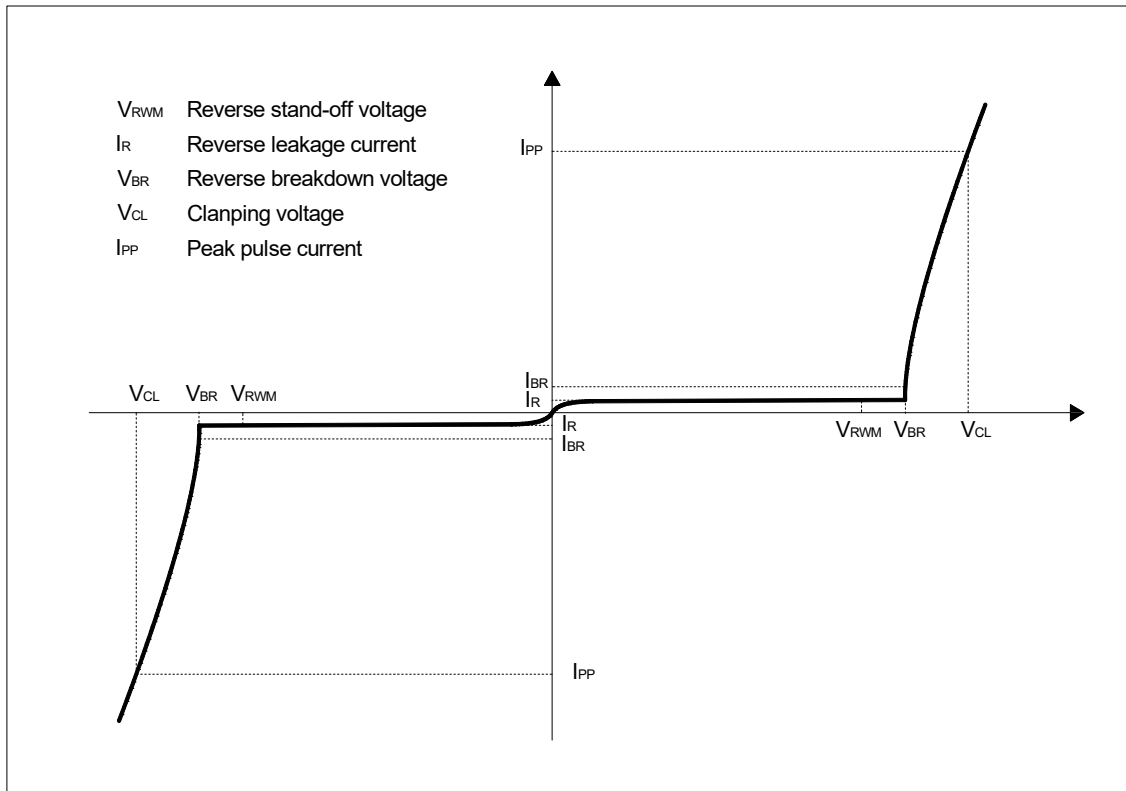
- Cellular Handsets and Accessories
- Display Ports
- MDDI Ports
- USB Ports
- Digital Visual Interface (DVI)
- PCI Express and Serial SATA Ports

Mechanical Data

- Package: DFN1006-2L
- Case Material: "Green" Molding Compound
- Marking Information: See Below



■Definitions of electrical characteristics





ESDSL5V0LBS2

■Maximum Ratings

PARAMETER	SYMBOL	LIMITS	UNIT
Peak pulse power ($t_p = 8/20\mu s$)	P_{pk}	45	W
Peak pulse current ($t_p = 8/20\mu s$)	I_{PP}	3	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	± 20	kV
ESD according to IEC61000-4-2 contact discharge		± 20	
Junction temperature	T_J	-55 to ~150	$^{\circ}C$
Storage temperature	T_{STG}	-55 to ~150	$^{\circ}C$

■Electrical Characteristics ($T_a=25^{\circ}C$ Unless otherwise specified)

PARAMETER	Symbol	UNIT	Conditions	Min	Typ	Max
Reverse maximum working voltage	V_{RWM}	V				5
Reverse breakdown voltage	V_{BR}	V	$I_{BR} = 1mA$	6		
Reverse leakage current	I_R	μA	$V_{RWM} = 5V$			0.2
Clamping voltage ³⁾	V_{CL}	V	$I_{PP} = 1A, t_p = 8/20\mu s$			11
		V	$I_{PP} = 3A, t_p = 8/20\mu s$			15
Junction capacitance	C_J	pF	$V_R = 0V, f = 1MHz$		0.15	0.25

Notes:

- (1). TLP parameter: $Z_0 = 50\Omega$, $t_p = 100ns$, $t_r = 2ns$, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.
- (2). Contact discharge mode, according to IEC61000-4-2.
- (3). Non-repetitive current pulse, according to IEC61000-4-5.

■Ordering Information (Example)

PREFERRED P/N	PACKING CODE	UNIT WEIGHT(mg)	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
ESDSL5V0LBS2	F1	Approximate 0.9	10000	100000	400000	7" reel



ESDLC5V0LBS2

■ Characteristics (Typical)

Fig.1 8/20 μ s waveform per IEC61000-4-5

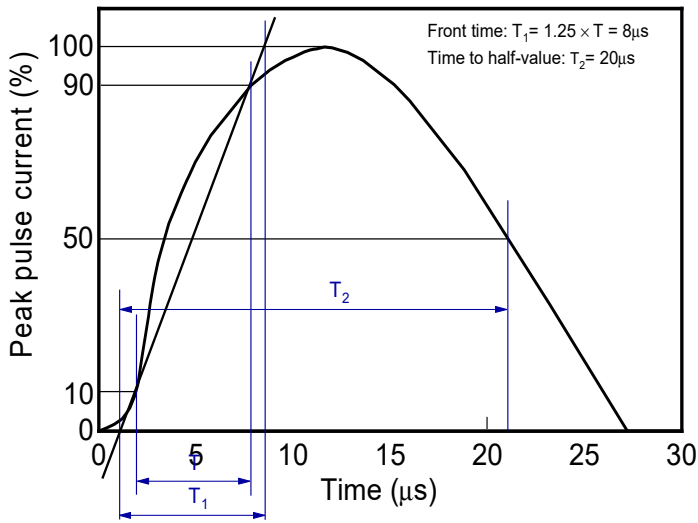


Fig.2 Contact discharge current waveform per IEC61000-4-2

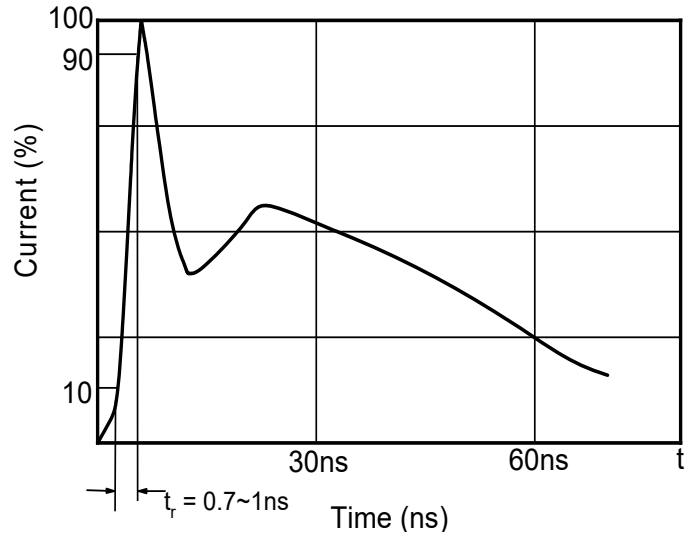


Fig.3 Clamping voltage vs. Peak pulse current

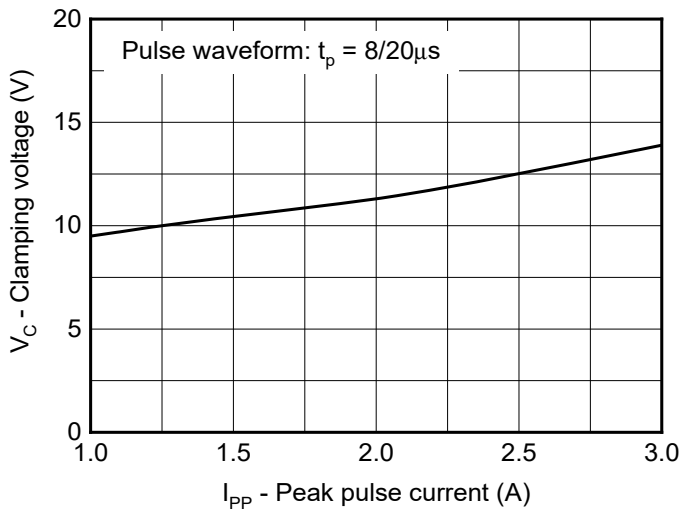


Fig.4 Capacitance vs. Reverse voltage

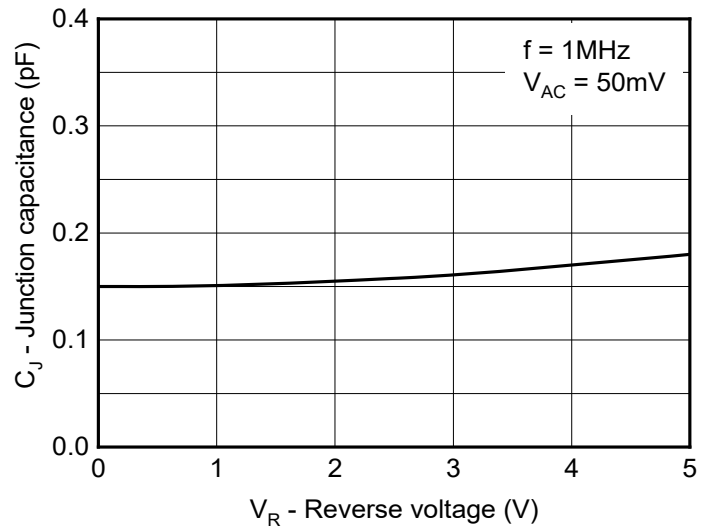


Fig.5 Non-repetitive peak pulse power vs. Pulse time

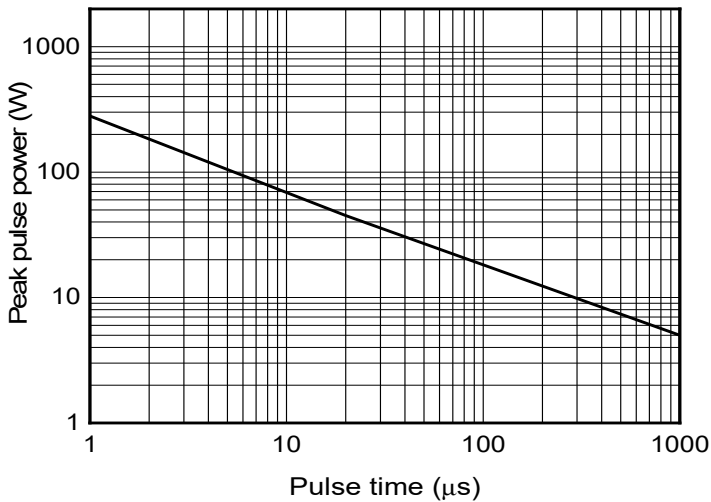


Fig.6 Power derating vs. Ambient temperature

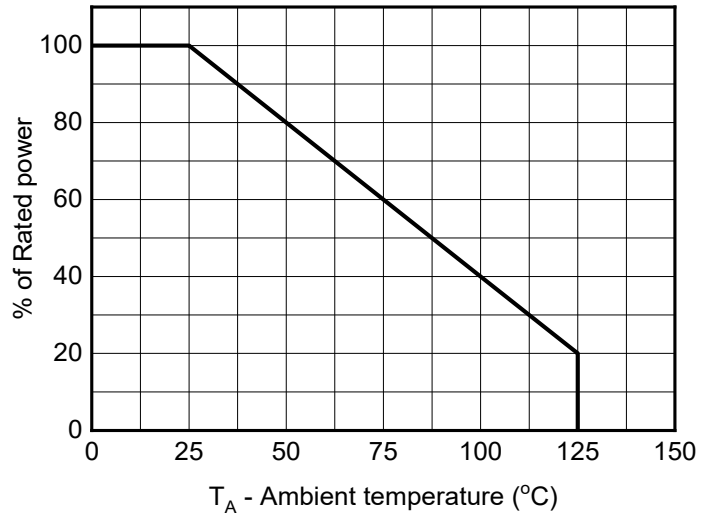
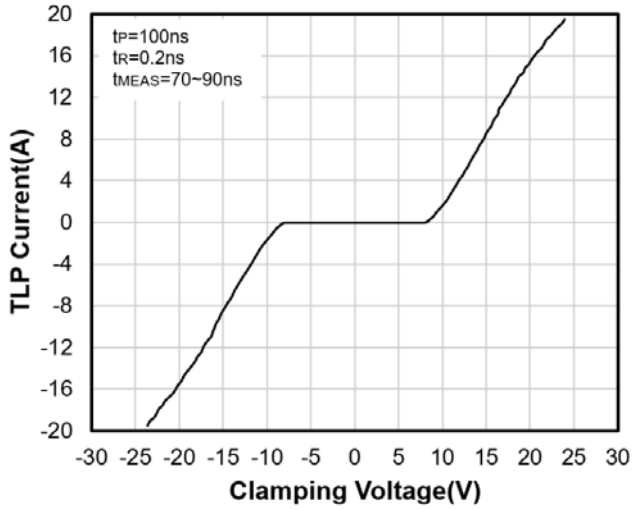




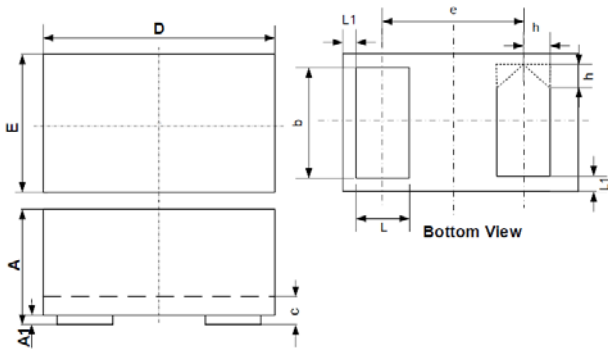
Fig.7 TLP Measurement





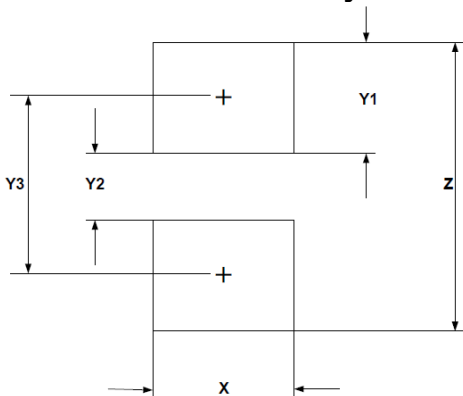
ESDSL5V0LBS2

■ Outline Dimensions



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.45	0.50	0.55	0.018	0.020	0.022
c	0.12	0.15	0.18	0.005	0.006	0.007
D	0.95	1.00	1.05	0.037	0.039	0.041
e	0.65 BSC			0.026 BSC		
E	0.55	0.60	0.65	0.022	0.024	0.026
L	0.20	0.25	0.30	0.008	0.010	0.012
L1	0.05REF			0.002REF		
h	0.07	0.12	0.17	0.003	0.005	0.007

■ Recommended PCB Layout



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
X	0.60	0.024
Y1	0.50	0.020
Y2	0.30	0.012
Y3	0.80	0.032
Z	1.30	0.052

Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met



ESDSL5V0LBS2

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