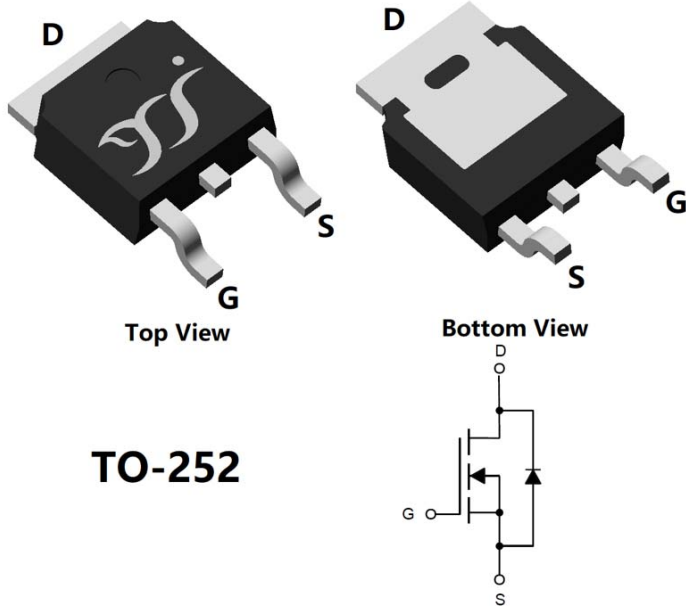


## N-Channel Enhancement Mode Field Effect Transistor



TO-252

### Product Summary

- $V_{DS}$  60V
- $I_D$  50A
- $R_{DS(ON)}$ ( at  $V_{GS}=10V$ )  $< 15m\Omega$
- $R_{DS(ON)}$ ( at  $V_{GS}=4.5V$ )  $< 18m\Omega$
- 100% EAS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Trench Power LV MOSFET technology
- High density cell design for low  $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

### Applications

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply
- DC-DC convertor
- 12V,24V Automotive systems

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	60	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_A=25^\circ C$	$I_D$	8.6	A
	$T_A=100^\circ C$		5.4	
	$T_C=25^\circ C$		50	
	$T_C=100^\circ C$		32	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	120	A
Avalanche energy <sup>B</sup>		EAS	72	mJ
Total Power Dissipation <sup>C</sup>	$T_A=25^\circ C$	$P_D$	2.5	W
	$T_A=100^\circ C$		1	
	$T_C=25^\circ C$		59.5	
	$T_C=100^\circ C$		23.8	
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	2.1	$^\circ C/W$
Thermal Resistance Junction-to-Ambient <sup>D</sup>		$R_{\theta JA}$	50	$^\circ C/W$
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ C$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD50N06AQ	F1	YJD50N06A	2500	/	25000	13"Reel



# YJD50N06AQ

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			± 100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =15A		11	15	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A		12.5	18	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =15A, V <sub>GS</sub> =0V		0.85	1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz		1.2		Ω
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz	-	2515	-	pF
Output Capacitance	C <sub>oss</sub>		-	165	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	130	-	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =20A	-	46	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	6	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	11	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =20A, di/dt=100A/us	-	28.2	-	nC
Reverse Recovery Time	t <sub>rr</sub>		-	32	-	ns
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =30V, I <sub>D</sub> =20A	-	9	-	ns
Turn-on Rise Time	t <sub>r</sub>		-	41	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	28	-	
Turn-off fall Time	t <sub>f</sub>		-	2.8	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T<sub>J</sub>=25°C, V<sub>DD</sub>=50V, V<sub>G</sub>=10V, R<sub>G</sub>=25Ω, L=0.5mH, I<sub>AS</sub>=17A.

C. P<sub>d</sub> is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in the still air environment with T<sub>A</sub> =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



# YJD50N06AQ

## Typical Electrical and Thermal Characteristics Diagrams

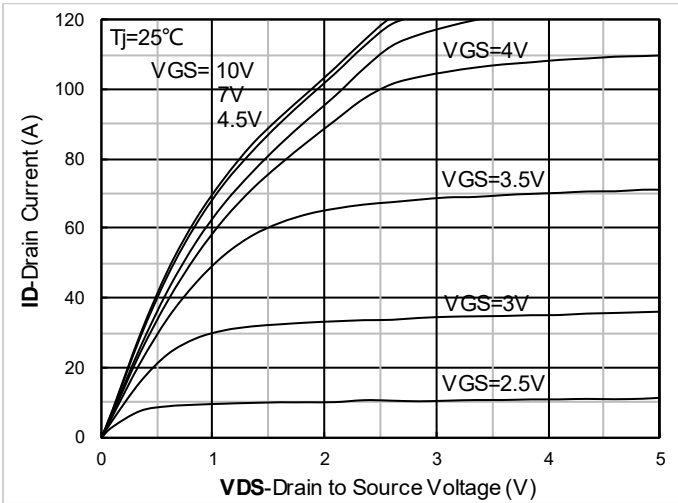


Figure 1. Output Characteristics

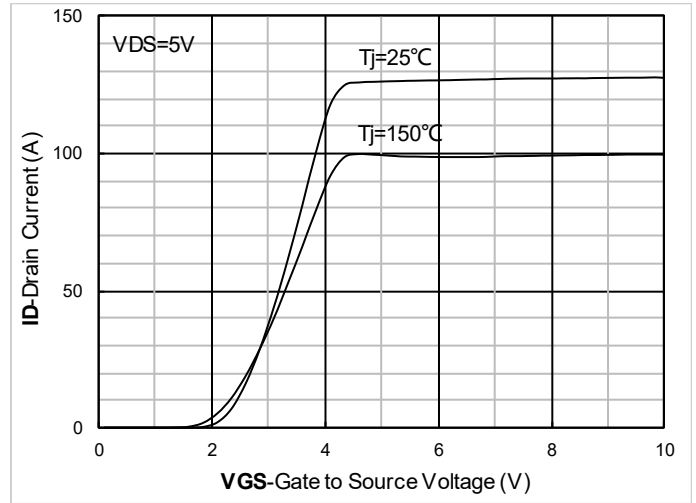


Figure 2. Transfer Characteristics

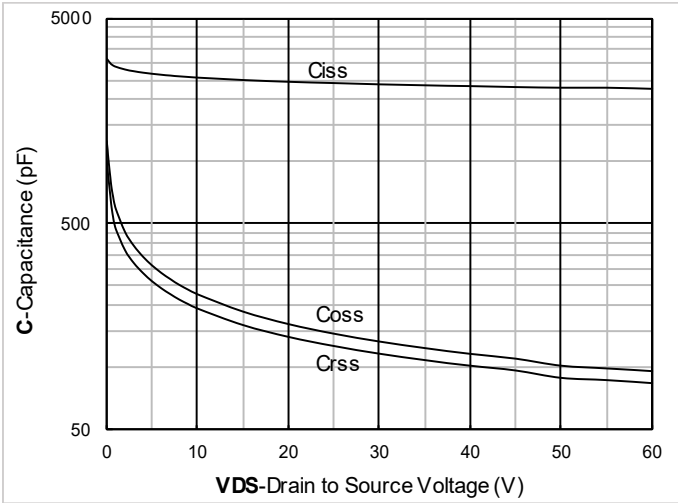


Figure 3. Capacitance Characteristics

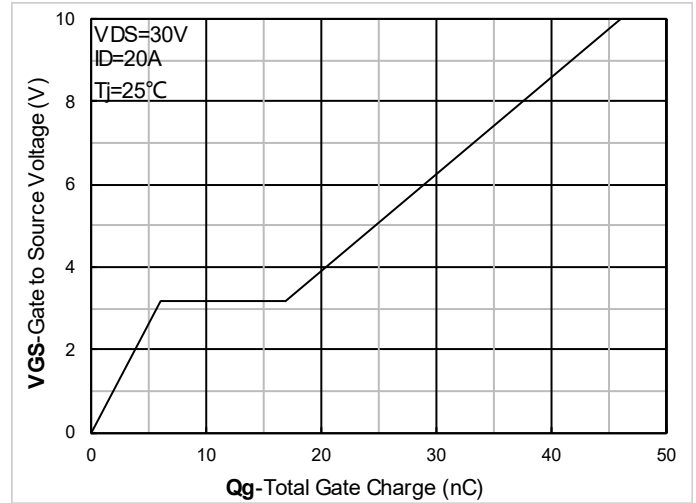


Figure 4. Gate Charge

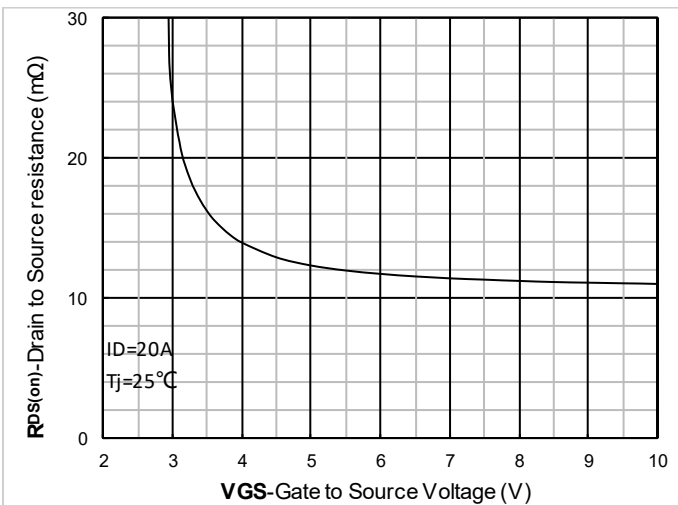


Figure 5. On-Resistance vs Gate to Source Voltage

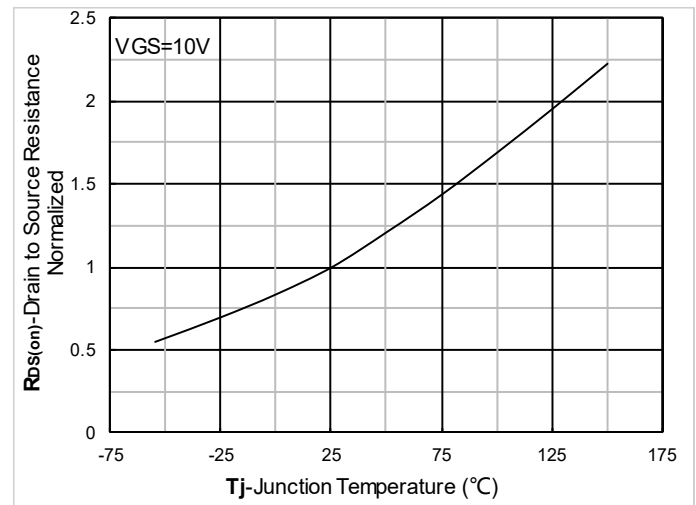


Figure 6. Normalized On-Resistance



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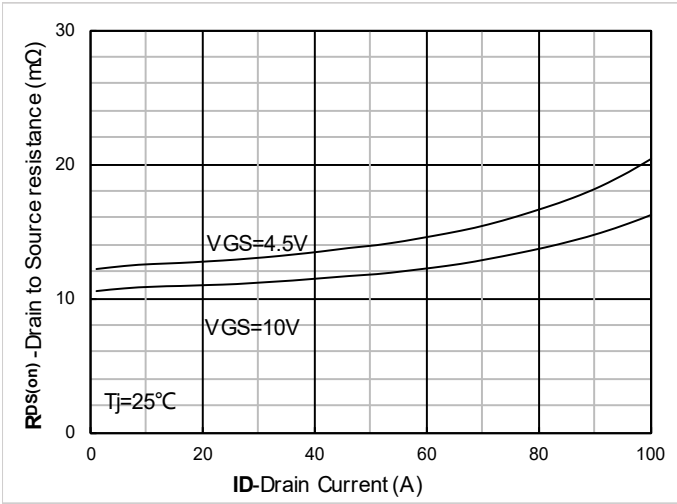


Figure 7.  $R_{DS(on)}$  VS Drain Current

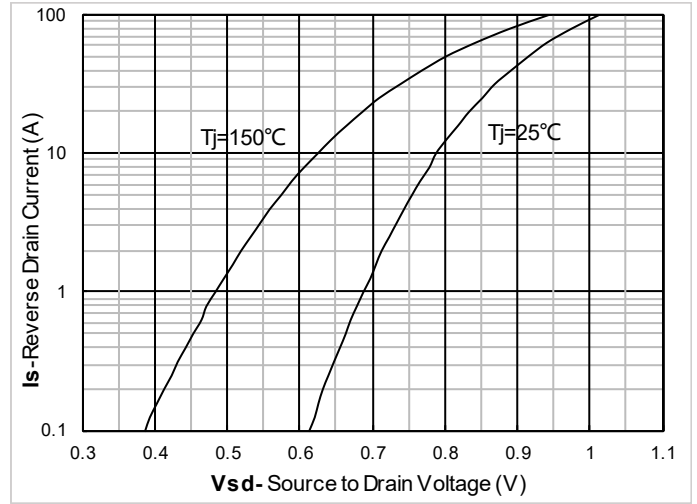


Figure 8. Forward characteristics of reverse diode

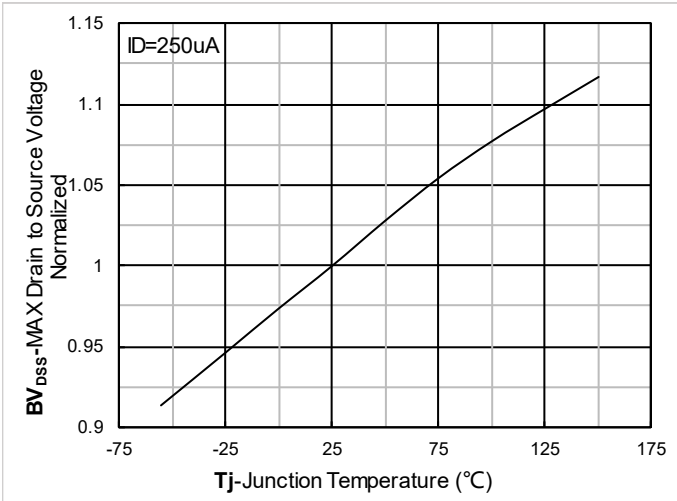


Figure 9. Normalized breakdown voltage

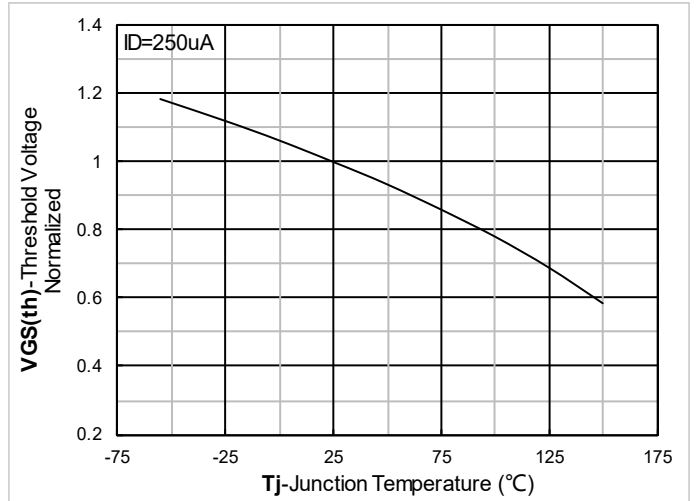


Figure 10. Normalized Threshold voltage

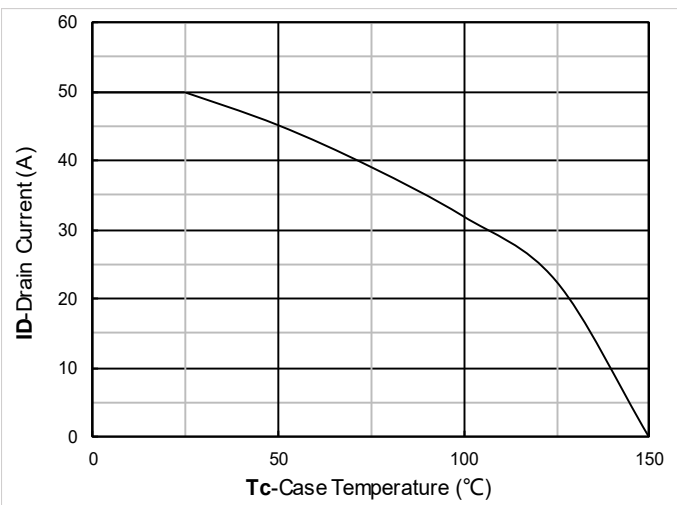


Figure 11. Current dissipation

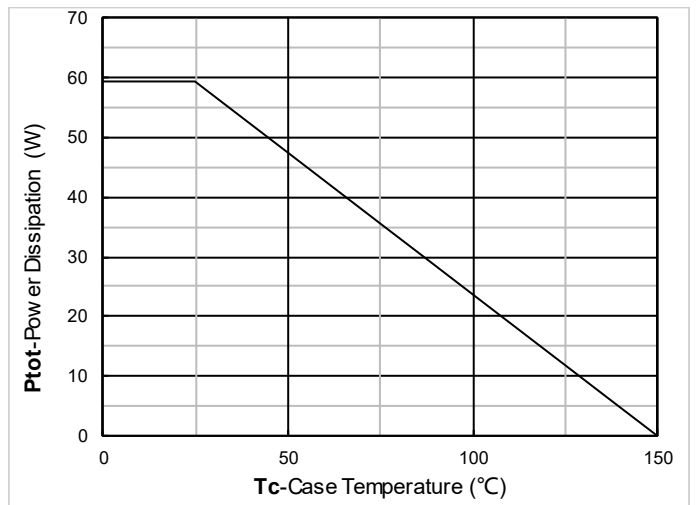


Figure 12. Power dissipation



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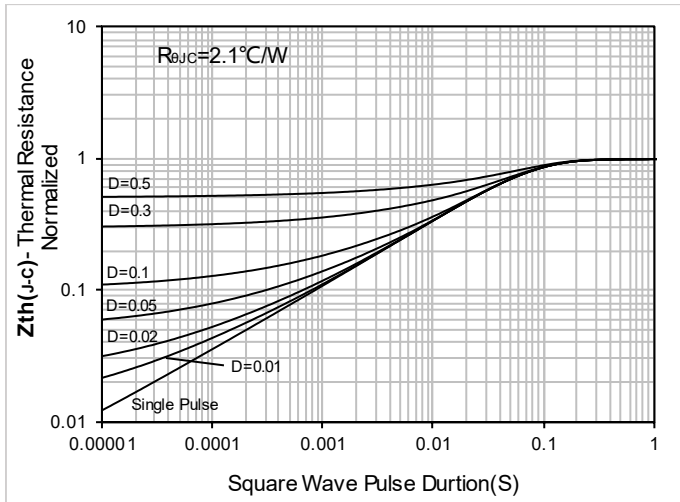


Figure 13. Maximum Transient Thermal Impedance

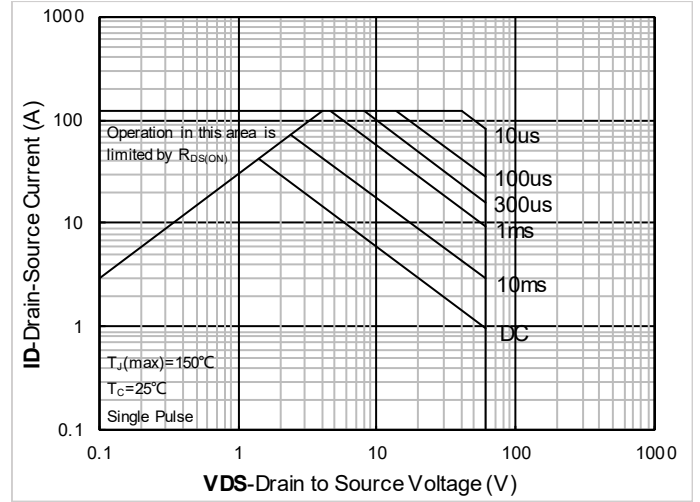
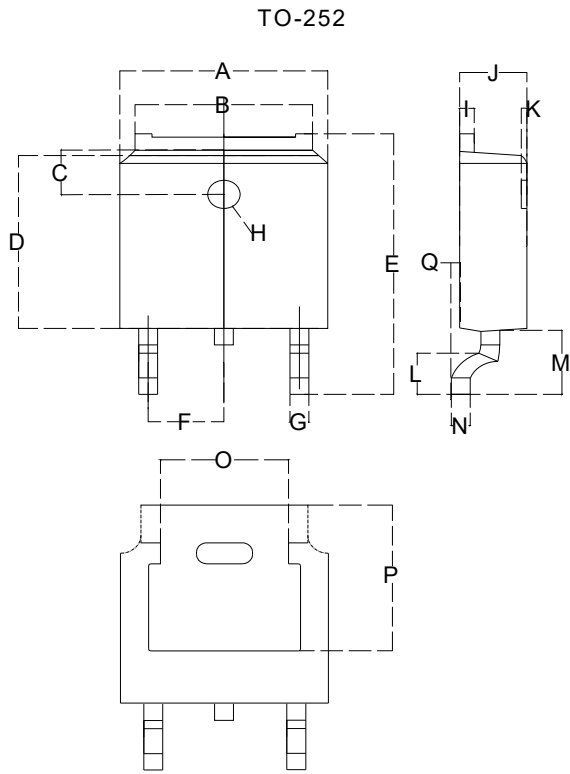


Figure 14. Safe Operation Area



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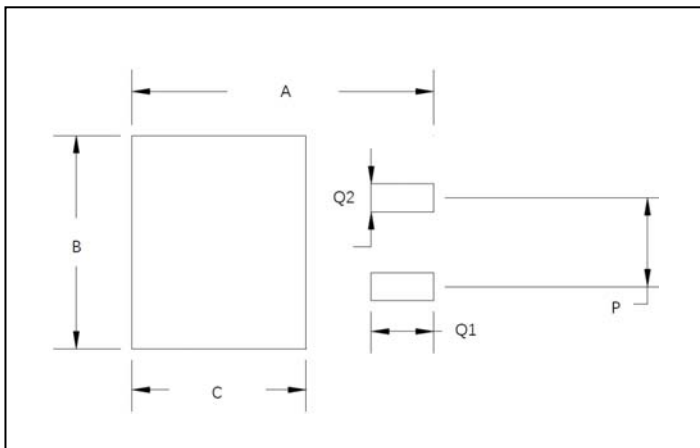
## ■ TO-252 Package information



Dimensions in millimeters

TO-252		
Dim	Min	Max
A	6.500	6.700
B	5.100	5.460
C	1.400	1.800
D	6.000	6.200
E	10.000	10.400
F	2.166	2.366
G	0.660	0.860
H	Φ1.050	Φ1.350
I	0.460	0.580
J	2.200	2.400
K	0	0.300
L	0.890	2.290
M	2.730	3.080
N	0.430	0.580
O	4.20	4.95
P	5.15	5.45
Q	0	0.2

## ■ Suggested Pad Layout



Dim	Millimeters
A	11.4
B	6.74
C	6.23
P	4.56
Q1	2.28
Q2	1.52



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