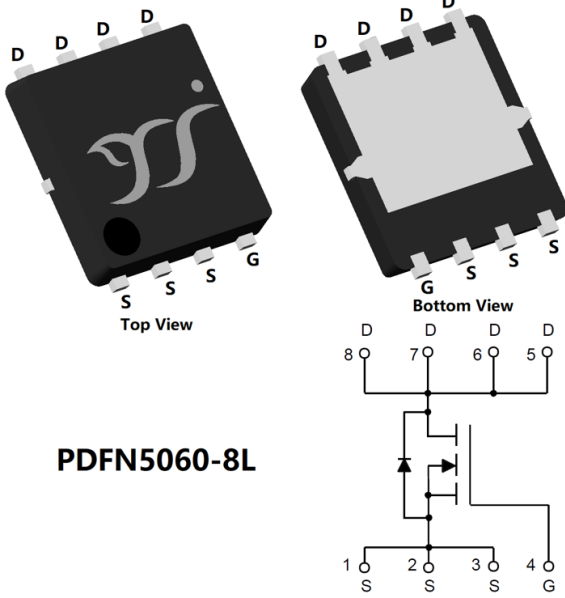


## N-Channel Enhancement Mode Field Effect Transistor



### Product Summary

- $V_{DS}$  40V
- $I_D$  180A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ )  $< 1.7m\Omega$
- 100% EAS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

### Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

### Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	40	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_C=25^\circ C$	$I_D$	180	A
	$T_C=100^\circ C$		126	
	$T_A=25^\circ C$		30	
	$T_A=100^\circ C$		22	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	500	A
Avalanche energy <sup>B</sup>		EAS	270	mJ
Total Power Dissipation <sup>C</sup>	$T_C=25^\circ C$	$P_D$	187	W
	$T_C=100^\circ C$		93	
	$T_A=25^\circ C$		3	
	$T_A=100^\circ C$		1.5	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+175	$^\circ C$

### Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State	$R_{\theta JA}$	40	50	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.65	0.8	

### Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG180G04HJRQ	F1	180G04HJR	5000	10000	100000	13" reel

■ Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=40V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	2.5	4	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$	-	1.3	1.7	m $\Omega$
Diode Forward Voltage	$V_{SD}$	$I_S=20A, V_{GS}=0V$	-	0.8	1.2	V
Gate resistance	$R_G$	$f=1\text{MHz}$	-	2	-	$\Omega$
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V, f=1\text{MHz}$	-	3300	-	pF
Output Capacitance	$C_{oss}$		-	1155	-	
Reverse Transfer Capacitance	$C_{rss}$		-	120	-	
<b>Switching Parameters</b>						
Total Gate Charge	$Q_g$	$V_{GS}=10V, V_{DS}=20V, I_D=90A$	-	60.8	-	nC
Gate-Source Charge	$Q_{gs}$		-	17	-	
Gate-Drain Charge	$Q_{gd}$		-	18	-	
Reverse Recovery Charge	$Q_{rr}$	$I_F=55A, di/dt=100A/\mu s$	-	23.5	-	nC
Reverse Recovery Time	$t_{rr}$		-	35.3	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=20V, I_D=90A$ $R_{GEN}=3\Omega$	-	14.5	-	ns
Turn-on Rise Time	$t_r$		-	38.2	-	
Turn-off Delay Time	$t_{D(off)}$		-	45.3	-	
Turn-off fall Time	$t_f$		-	31.6	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B.  $T_J=25^\circ\text{C}$ ,  $V_{DD}=30V$ ,  $V_G=10V$ ,  $R_G=25\Omega$ ,  $L=0.5\text{mH}$ ,  $I_{AS}=32.9A$ .

C.  $P_d$  is based on max. junction temperature, using junction-case thermal resistance.

D. The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in the still air environment with  $T_A=25^\circ\text{C}$ . The maximum allowed junction temperature of  $175^\circ\text{C}$ . The value in any given application depends on the user's specific board design.

## Typical Electrical and Thermal Characteristics Diagrams

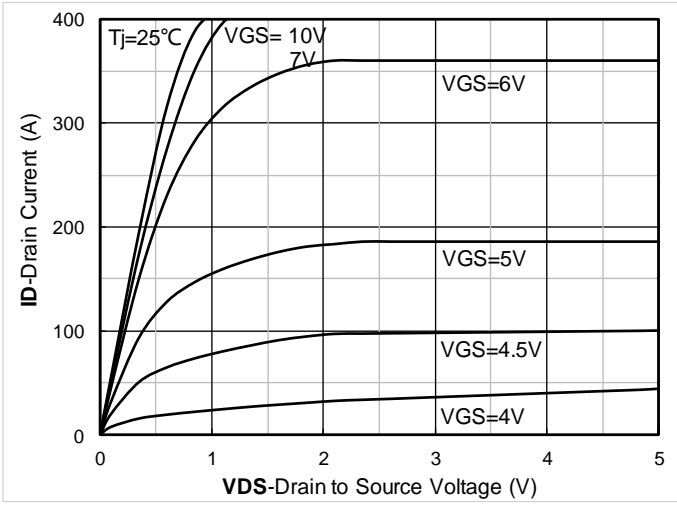


Figure 1. Output Characteristics

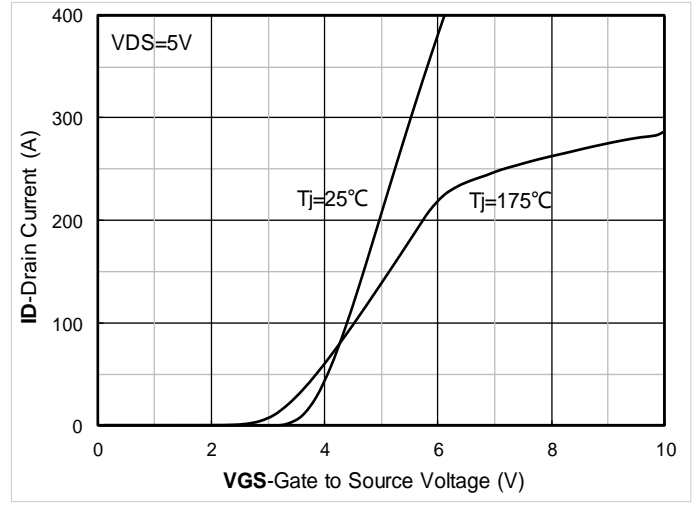


Figure 2. Transfer Characteristics

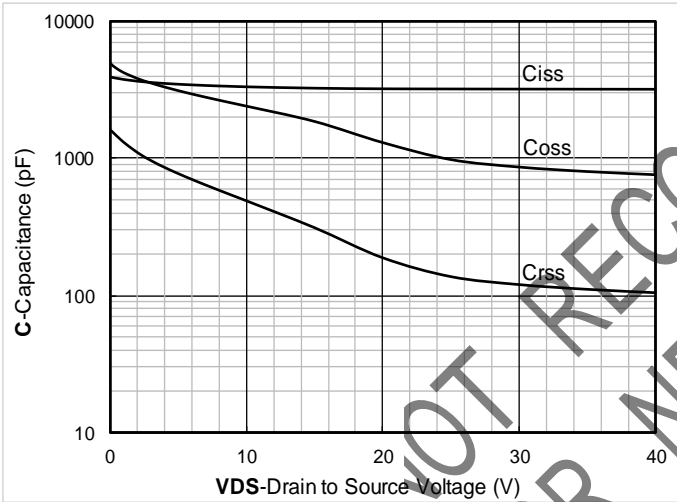


Figure 3. Capacitance Characteristics

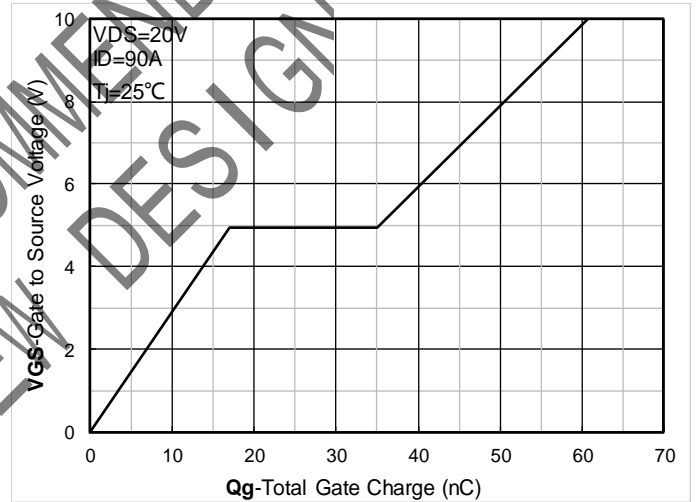


Figure 4. Gate Charge

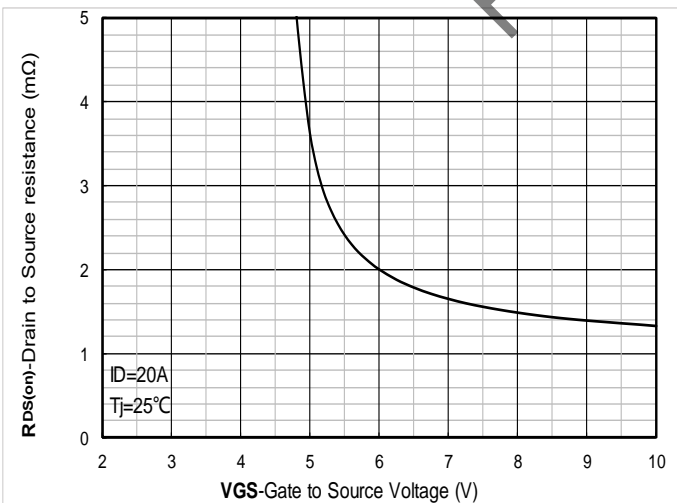


Figure 5. On-Resistance vs Gate to Source Voltage

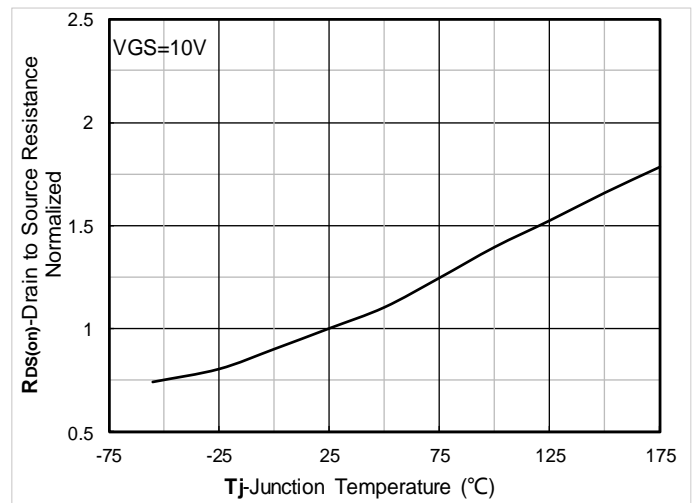


Figure 6. Normalized On-Resistance

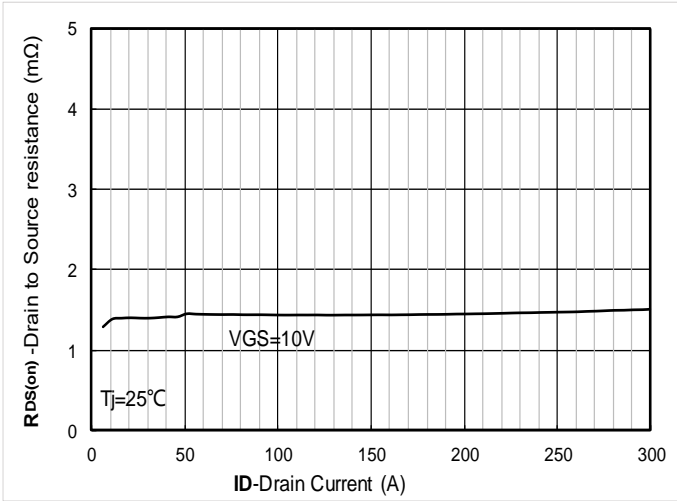


Figure 7. RDS(on) VS Drain Current

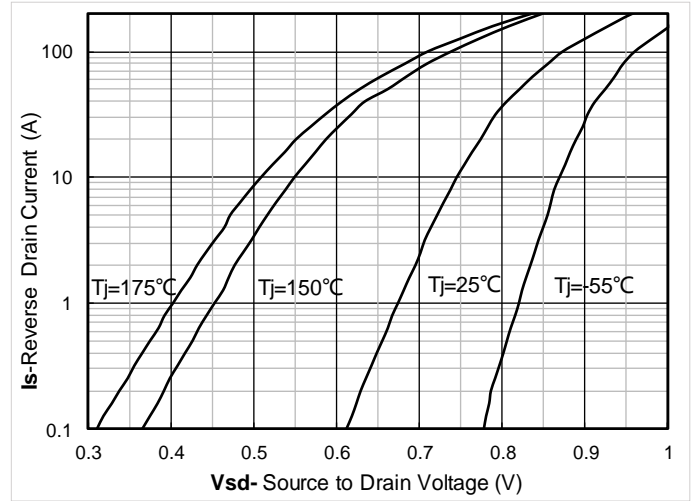


Figure 8. Forward characteristics of reverse diode

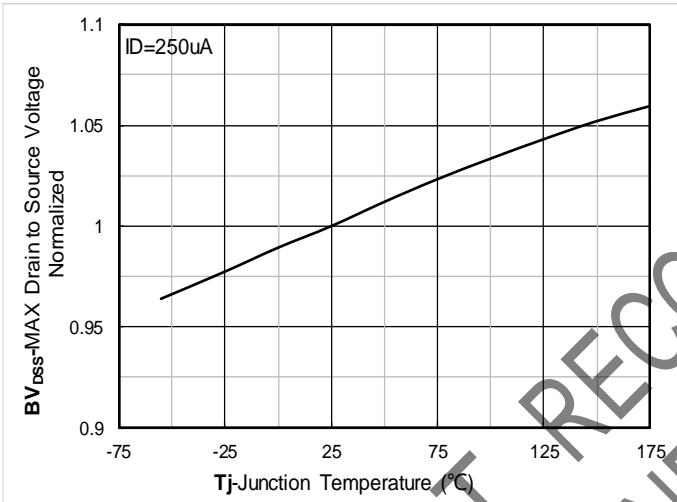


Figure 9. Normalized breakdown voltage

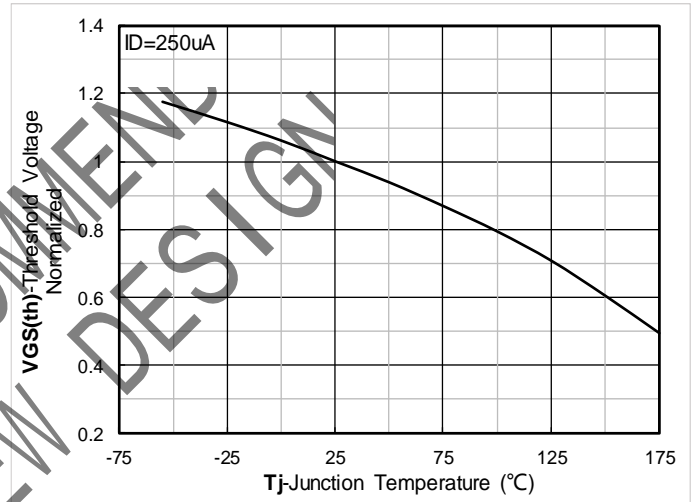


Figure 10. Normalized Threshold voltage

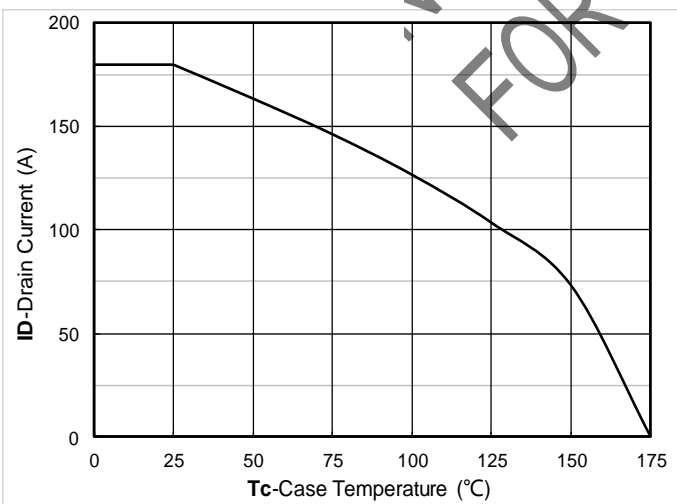


Figure 11. Current dissipation

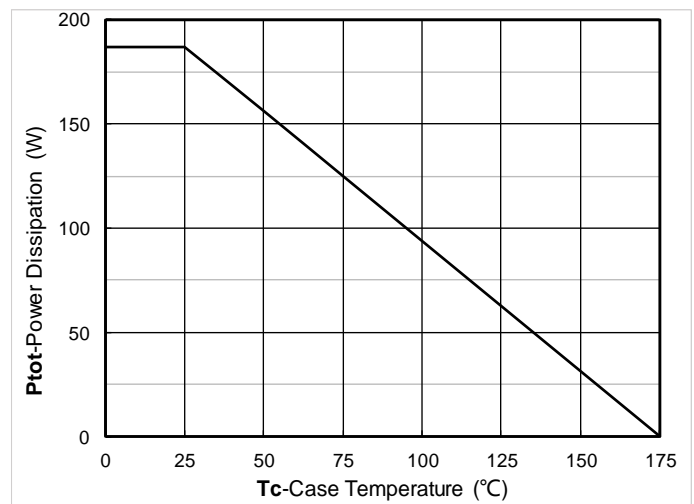


Figure 12. Power dissipation

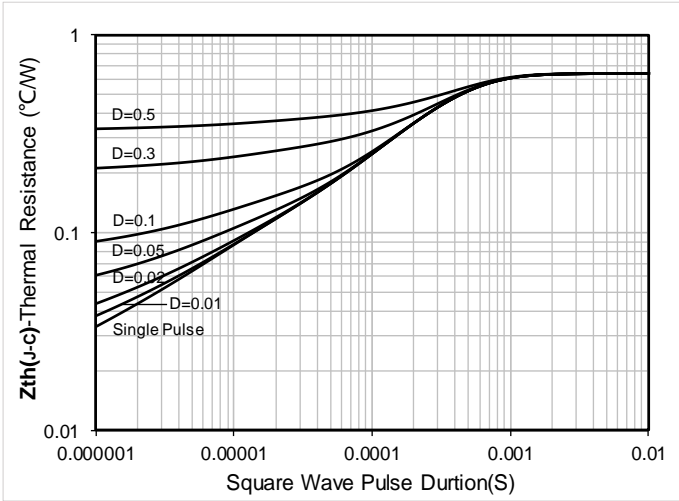


Figure 13. Maximum Transient Thermal Impedance

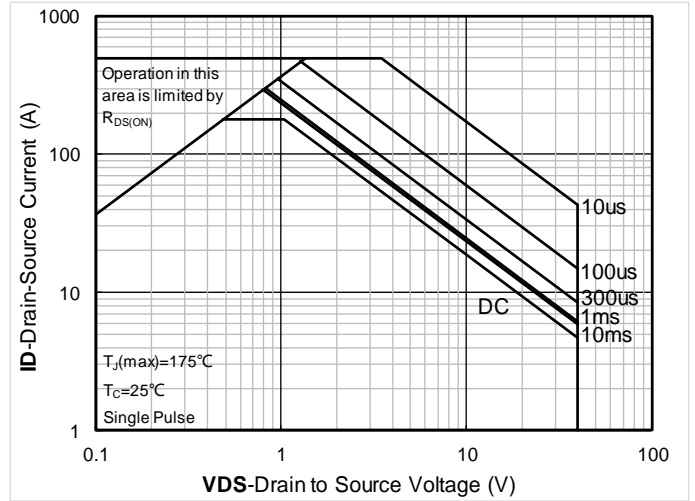


Figure 14. Safe Operation Area

## ■ Test Circuits & Waveforms

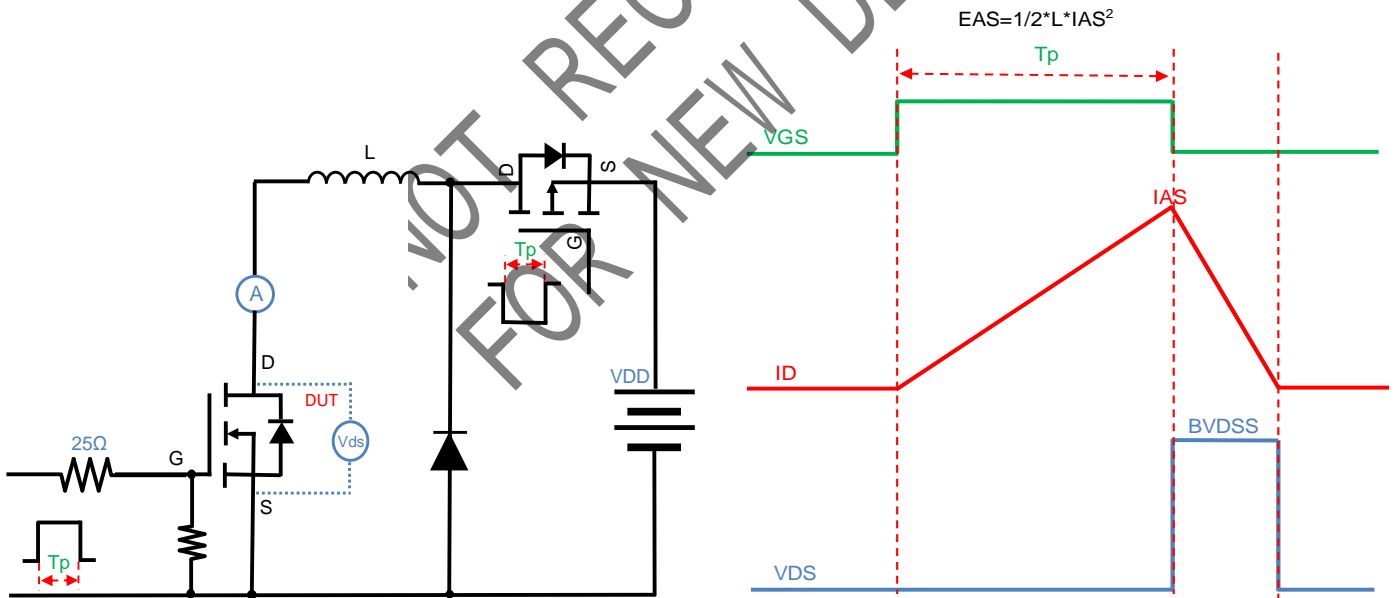


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

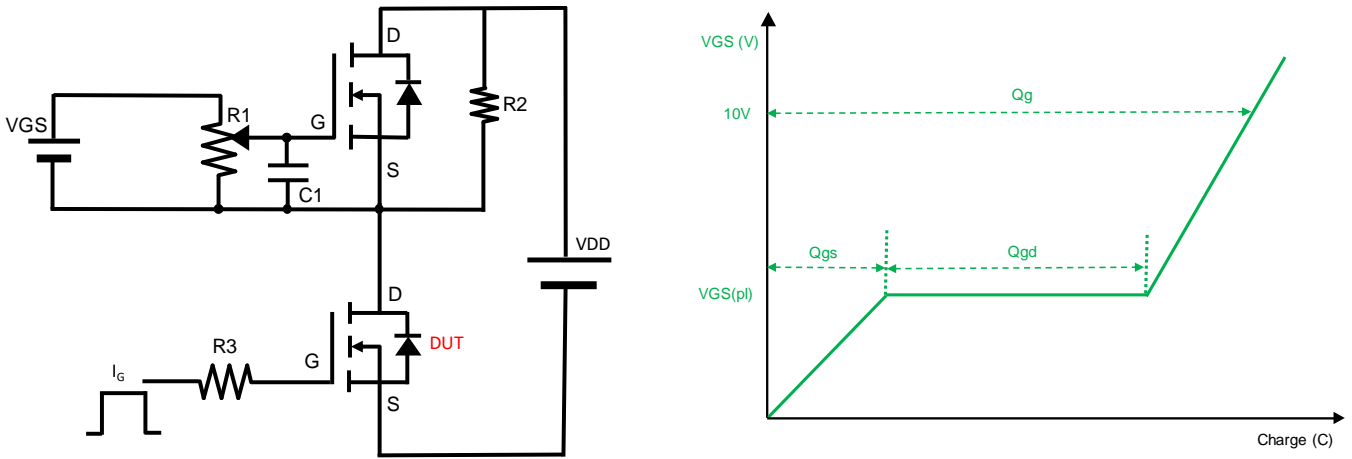


Figure B. Gate Charge Test Circuit & Waveform

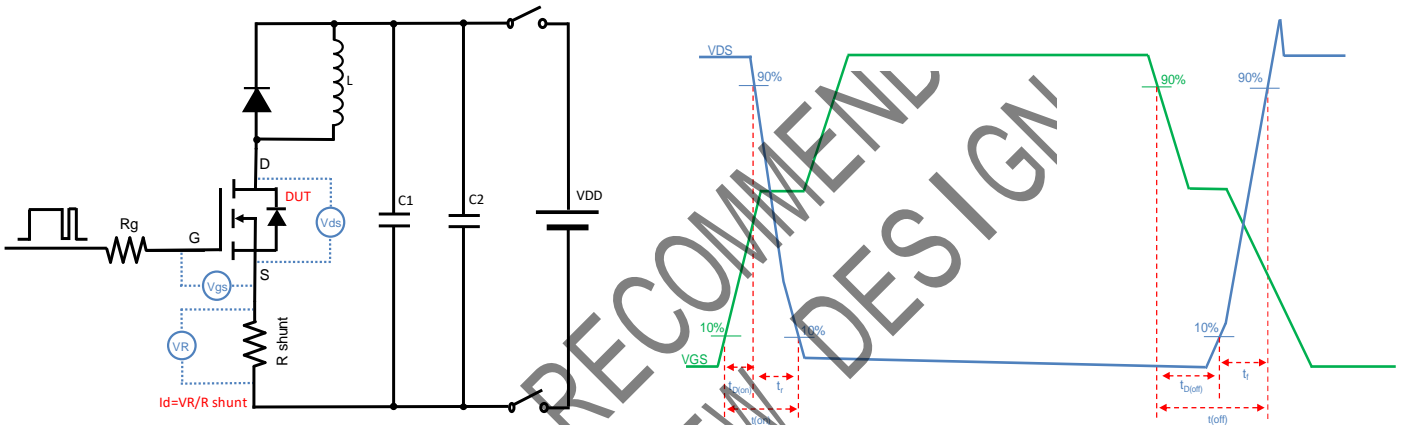


Figure C. Resistive Switching Test Circuit & Waveform

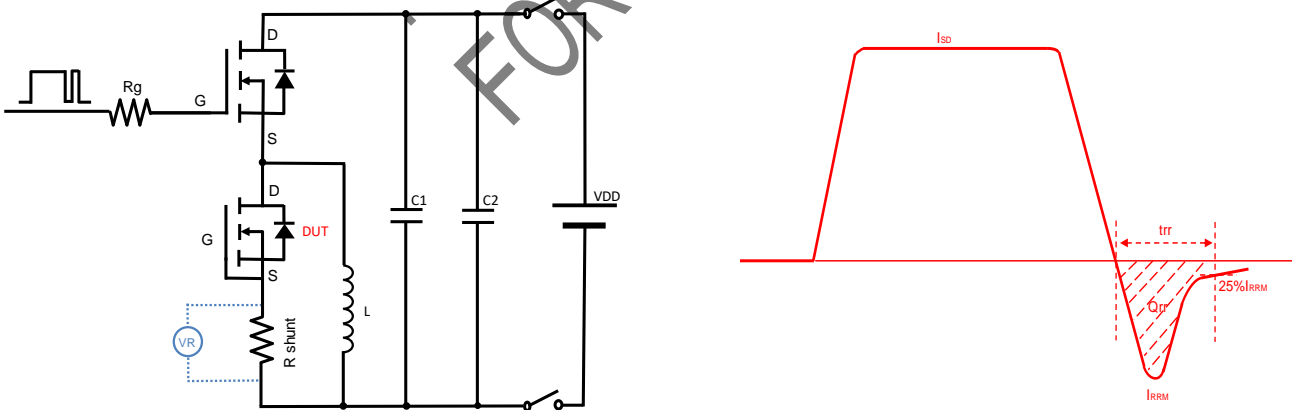


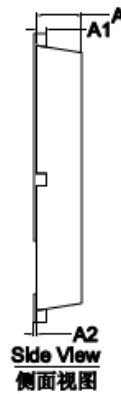
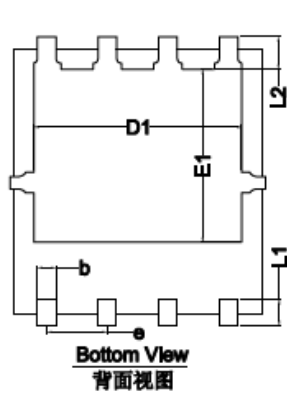
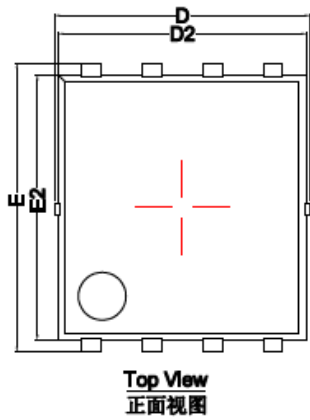
Figure D. Diode Recovery Test Circuit & Waveform



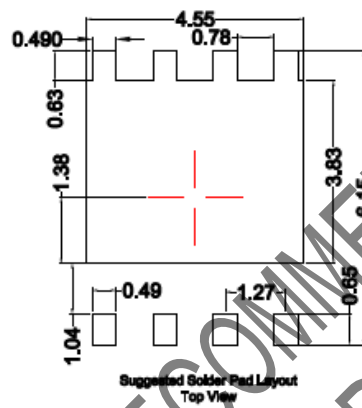
# YJG180G04HJRQ

RECOMMEND  
YJG1D7G04HRQ  
FOR NEW DESIGN

## ■ PDFN5060-8L-0.95MM Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.05	6.15
A	0.85	0.95	1.05
A1	0.203 BSC		
A2			0.08
D1	4.25	4.35	4.45
E1	3.525	3.625	3.725
D2		5.20	
E2		5.55	
L1	0.45	0.55	0.65
L2	0.68 BSC		
b	0.3	0.4	0.5
e	1.27 BSC		



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance:  $\pm 0.10$ mm.  
 3. The pad layout is for reference purposes only.

NOT RECOMMEND  
FOR NEW DESIGN



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